Seminar

HPC Lab · CDS

Center for Data and Simulation Science

Wednesday, May 10, 2023
4–5:30 p.m.
Seminar Room 1
Mathematical Institute
University of Cologne
Weyertal 86–90

Speaker:

Pierre-Edouard Beaucamps
System Application Manager
Kalray

INTRODUCING KALRAY DPU

A MANYCORE PROCESSOR DESIGNED FOR PERFORMANCE & FLEXIBILITY

The world is facing an explosion of data, bringing new processing challenges. Every day, new algorithms are developed and run on high-performance processors to sustain the computational requirements, which often means going with GPUs.
But technologies developed decades ago are not always able to handle these massive workloads efficiently, especially in terms of real-time processing, power consumption, heterogeneous multiprocessing, or freedom-from-interference.
Although originally designed for graphics processing, GPUs are indeed very effective at providing high-level computing capabilities, but their architecture can also prevent applications from taking full advantage of their capabilities.
This presentation will introduce a new type of processor designed by Kalray, the MPPA® DPU (Data Processing Unit), based on a unique manycore architecture.
Kalray DPU is a high-performance, low-power programmable processor, capable of competing with GPUs, DSPs, and FPGAs, offering a high level of performance at a competitive cost, and beyond that, one of the best performance per watt ratio available in the market.
Based on the lessons learned from the past, current developments and promises are evaluated in order to derive an outlook, where the implementation of DPUs provides comprehensive advantages in the education and research environment. We will provide a deeper insight, which applications will benefit from DPUs and how a collaboration between University of Cologne and Kalray could look like.

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